this opening would normally expose a diffusion region conductively doped into a starting substrate). Contact opening 22 not only allows access to the underlying topography but also provides a form for a subsequent placed layer of thin poly. This thin poly is now formed, preferably by CVD, as a layer of conformal polysilicon 23 and is placed overlying planarized oxide 21, the patterned edges of oxide 21 and the exposed underlying topography. Poly 23 may either have been deposited insitu doped or deposited insitu doped and rugged HSG poly for added cell capacitance or it may be subsequently doped.

Referring now to FIG. 3, a thick layer of oxide 31 having a high etch rate is formed over poly 23. Oxide 31 is thick enough to completely fill the poly lined contact opening 22.

Referring now to FIG. 4, oxide layer 31 is removed down to poly 23, preferably by CMP which will selectively stop on the first exposed upper regions of poly 23.

Referring now to FIG. 5, the exposed upper portions of poly 23 are removed to separate neighboring poly structures thereby forming individual containers 51 residing in contact openings 22 and exposing underlying oxide 21. The areas of poly 23 that are removed may be accomplished by performing a poly etch selective to oxide, which could be a timed wet etch or an optimized CMP poly etch. A very significant advantage of this process flow when a CMP etch step is utilized is that the inside of the future container 51 is protected from 'slurry' contamination that is inherent in the CMP step which proves difficult to remove in high aspect ratio storage containers (0.5μ inside diameter by 1.5μ high).

Referring now to FIG. 6, both oxides 21 and 31, which have different etch rates, are now exposed. At this point, an oxide etch is performed such that oxide 31 is completely removed from inside container 51 while a portion of oxide 21 remains at the base of container 51 and thereby providing an insulating layer between the underlying topography and subsequent layers. A etch rate ratio of 2:1 or greater between (a ratio of 4:1 is preferred) oxide 31 and oxide 22 provides sufficient process margin to ensure all of high etch rate oxide 31 inside container 51 is removed during the single etch step, while a portion of oxide 22 remains to provide adequate insulation from subsequently formed layers.

Referring now to FIG. 7, when using this structure to form a capacitor storage node plate container 51 and the remaining portion of oxide 21 is coated with a capacitor cell dielectric 71. And, finally a second conformal poly layer 72 is placed to blanket cell dielectric 71 and serves as a common capacitor cell plate to the entire array of containers 51. From this point on the wafer is completed using conventional fabrication process steps.

FIG. 8 depicts a cross-section of the present invention integrated into a stacked capacitor process on starting substrate 81. Container 51 connects to diffusion area 82 and thereby serves as a storage node container plate. Diffusion area 82 is accessed by word line 85 (separated by gate insulator 83) which in turn spans the channel's active area between diffusion areas 82. The poly of container 51 is doped to the same conductivity type as underlying diffusion region 82 to insure a good ohmic contact.

It is to be understood that although the present invention has been described with reference to a preferred embodiment, various modifications, known to those skilled in the art, may be made to the structures and process steps presented herein without departing from the invention as recited in the several claims appended hereto.

We claim:

1. A process for fabricating a uniform and repeatable conductive container structure on a starting substrate's existing topography, said process comprising the steps of:

a) forming a blanketing first insulating layer, having a first etch rate, over said existing topography;

b) patterning and etching an opening into said first insulating layer, said opening thereby forming a container form;

c) forming a conformal first conductive layer superjacent said first insulating layer and said container form thereby lining said container form;

d) forming a blanketing second insulating layer, having a second etch rate, superjacent said first conductive layer;

e) removing said second insulating layer via chemical mechanical planarization until upper portion of said first conductive layer is exposed;

f) removing said exposed first conductive upper layer until underlying said first insulating layer is exposed thereby separating said first conductive layer into individual said conductive containers having inner and outer walls;

g) removing said first and said second insulating layers such that said second insulating layer is completely removed thereby exposing the entire inner walls of said conductive container and said first insulating layer is partially removed thereby exposing an upper portion of said outer walls of said conductive container, wherein the partially remaining first insulating layer provides insulation between said underlying substrate topography and subsequently formed layers;

h) forming a third insulating layer superjacent and coextensive said exposed walls and inner bottom portion of said container and said partially remaining first insulating layer; and

i) forming a second conductive layer superjacent and coextensive said third insulating layer.

2. A process as recited in claim 1, wherein said first insulating layer is planarized prior to said step of patterning and etching an opening into said first insulating layer.

3. A process as recited in claim 1, wherein said second insulating layer is a sacrificial layer conducive to said chemical mechanical planarization.

4. A process as recited in claim 1, wherein said first and said second insulating layers are oxides.

5. A process as recited in claim 1, wherein said first insulating layer etch rate is a lower etch rate than said second insulating layer etch rate.

6. A process as recited in claim 5, wherein the etch rate ratio between said second insulating layer etch rate and said first insulating layer etch rate is a ratio of 2:1 or greater.

7. A process as recited in claim 5, wherein the etch rate ratio between said second insulating layer etch rate and said first insulating layer etch rate is a ratio of 4:1.

8. A process as recited in claim 1, wherein said first and said second conductive layers are doped polysilicon.

9. A process as recited in claim 8, wherein said doped polysilicon is formed by insitu doped chemical vapor deposition.

10. A process as recited in claim 1, wherein said first, said second and said third insulating layers are formed by chemical vapor deposition.

11. A process for fabricating a uniform and repeatable conductive container structure on a starting substrate's existing topography, said process comprising the steps of:

a) forming a blanketing first insulating layer, having a first etch rate, over said existing topography;
b) patterning and etching an opening into said first insulating layer, said opening thereby forming a container form;
c) forming a conformal first conductive layer superjacent said first insulating layer and said container form thereby lining said container form;
d) forming a blanketing second insulating layer, having a second etch rate, superjacent said first conductive layer;
e) removing said second insulating layer until upper portion of said first conductive layer is exposed;
f) removing said exposed first conductive upper layer via chemical mechanical planarization until underlying said first insulating layer is exposed thereby separating said first conductive layer into individual said conductive containers having inner and outer walls;
g) removing said first and said second insulating layers such that said second insulating layer is completely removed thereby exposing the entire inner walls of said conductive container and said first insulating layer is partially removed thereby exposing an upper portion of said outer walls of said conductive container, wherein the partially remaining first insulating layer provides insulation between said underlying substrate topography and subsequently formed layers;
h) forming a third insulating layer superjacent and coextensive said exposed walls and inner bottom portion of said container and said partially remaining first insulating layer; and
i) forming a second conductive layer superjacent and coextensive said third insulating layer.

12. A process as recited in claim 1, wherein said first insulating layer is planarized prior to said step of patterning and etching an opening into said first insulating layer.

13. A process as recited in claim 1, wherein said second insulating layer is a sacrificial layer that is planarized by chemical mechanical planarization.

14. A process as recited in claim 1, wherein said first and said second insulating layers are oxides.

15. A process as recited in claim 1, wherein said first insulating layer etch rate is a lower etch rate than said second insulating layer etch rate.

16. A process as recited in claim 15, wherein the etch rate ratio between said second insulating layer etch rate and said first insulating layer etch rate is a ratio of 2:1 or greater.

17. A process as recited in claim 15, wherein the etch rate ratio between said second insulating layer etch rate and said first insulating layer etch rate is a ratio of 4:1.

18. A process as recited in claim 1, wherein said first and said second conductive layers are doped polysilicon.

19. A process as recited in claim 18, wherein said doped polysilicon is formed by insitu doped chemical vapor deposition.

20. A process as recited in claim 1, wherein said first, said second and said third insulating layers are formed by chemical vapor deposition.

21. A process for fabricating a uniform and repeatable conductive container structure on a starting substrate's existing topography, said process comprising the steps of:

a) forming a blanketing first insulating layer, having a first etch rate, over said existing topography;
b) patterning and etching an opening into said first insulating layer, said opening thereby forming a container form;
c) forming a conformal first conductive layer superjacent said first insulating layer and said container form thereby lining said container form;
d) forming a blanketing second insulating layer, having a second etch rate, superjacent said first conductive layer;
e) removing said second insulating layer via chemical mechanical planarization until upper portion of said first conductive layer is exposed;
f) removing said exposed first conductive upper layer via chemical mechanical planarization until underlying said first insulating layer is exposed thereby separating said first conductive layer into individual said conductive containers having inner and outer walls;
g) removing said first and said second insulating layers such that said second insulating layer is completely removed thereby exposing the entire inner walls of said conductive container and said first insulating layer is partially removed thereby exposing an upper portion of said outer walls of said conductive container, wherein the partially remaining first insulating layer provides insulation between said underlying substrate topography and subsequently formed layers;
h) forming a third insulating layer superjacent and coextensive said exposed walls and inner bottom portion of said container and said partially remaining first insulating layer; and
i) forming a second conductive layer superjacent and coextensive said third insulating layer.

22. A process as recited in claim 21, wherein said first insulating layer is planarized prior to said step of patterning and etching an opening into said first insulating layer.

23. A process as recited in claim 21, wherein said second insulating layer is a sacrificial layer conducive to said chemical mechanical planarization.

24. A process as recited in claim 21, wherein said first and said second insulating layers are oxides.

25. A process as recited in claim 21, wherein said first insulating layer etch rate is a lower etch rate than said second insulating layer etch rate.

26. A process as recited in claim 25, wherein the etch rate ratio between said second insulating layer etch rate and said first insulating layer etch rate is a ratio of 2:1 or greater.

27. A process as recited in claim 25, wherein the etch rate ratio between said second insulating layer etch rate and said first insulating layer etch rate is a ratio ob 4:1.

28. A process as recited in claim 21, wherein said first and said second conductive layers are doped polysilicon.

29. A process as recited in claim 28, wherein said doped polysilicon is formed by insitu doped chemical vapor deposition.

30. A process as recited in claim 21, wherein said first, said second and said third insulating layers are formed by chemical vapor deposition.

31. A process for fabricating a DRAM container storage capacitor on a silicon substrate having active areas, word lines and digit lines, said process comprising the following sequence of steps:

a) forming a blanketing first insulating layer, having a first etch rate, over said existing topography;
b) patterning and etching an opening into said first insulating layer, said opening thereby forming a container form;
c) forming a conformal first conductive layer superjacent said first insulating layer and said container form thereby lining said container form;
d) forming a blanketing second insulating layer, having a second etch rate, superjacent said first conductive layer;
e) removing said second insulating layer via chemical mechanical planarization until upper portion of said first conductive layer is exposed;
f) removing said exposed first conductive upper layer until underlying said first insulating layer is exposed thereby separating said first conductive layer into individual said container storage capacitors having inner and outer walls;
g) removing said first and said second insulating layers such that said second insulating layer is completely removed thereby exposing the entire inner walls of said container storage capacitor and said first insulating layer is partially removed thereby exposing an upper portion of said outer walls of said container storage capacitor, wherein the partially remaining first insulating layer provides insulation between said underlying substrate topography and subsequently formed layers;
h) forming a third insulating layer superjacent and coextensive said exposed walls and inner bottom portion of said capacitor and said partially remaining first insulating layer; and
i) forming a second conductive layer superjacent and coextensive said third insulating layer.

32. A process as recited in claim 31, wherein said first insulating layer is planarized prior to said step of patterning and etching an opening into said first insulating layer.

33. A process as recited in claim 31, wherein said second insulating layer is a sacrificial layer conductive to said chemical mechanical planarization.

34. A process as recited in claim 31, wherein said first and said second insulating layers are oxides.

35. A process as recited in claim 31, wherein said first insulating layer etch rate is a lower etch rate than said second insulating layer etch rate.

36. A process as recited in claim 35, wherein the etch rate ratio between said second insulating layer etch rate and said first insulating layer etch rate is a ratio of 2:1 or greater.

37. A process as recited in claim 35, wherein the etch rate ratio between said second insulating layer etch rate and said first insulating layer etch rate is a ratio of 4:1.

38. A process as recited in claim 31, wherein said first and said second conductive layers are doped polysilicon.

39. A process as recited in claim 38, wherein said doped polysilicon is formed by insitu doped chemical vapor deposition.

40. A process as recited in claim 31, wherein said first, said second and said third insulating layers are formed by chemical vapor deposition.

41. A process for fabricating a DRAM container storage capacitor on a silicon substrate having active areas, word lines and digit lines, said process comprising the following sequence of steps:

a) forming a blanketing first insulating layer, having a first etch rate, over said existing topography;
b) patterning and etching an opening into said first insulating layer, said opening thereby forming a container form;
c) forming a conformal first conductive layer superjacent said first insulating layer and said container form thereby lining said container form.
d) forming a blanketing second insulating layer, having a second etch rate, superjacent said first conductive layer;
e) removing said second insulating layer until upper portion of said first conductive layer is exposed;
f) removing said exposed first conductive upper layer via chemical mechanical planarization until underlying said first insulating layer is exposed thereby separating said first conductive layer into individual said container storage capacitors having inner and outer walls;
g) removing said first and said second insulating layers such that said second insulating layer is completely removed thereby exposing the entire inner walls of said container storage capacitor and said first insulating layer is partially removed thereby exposing an upper portion of said outer walls of said container storage capacitor, wherein the partially remaining first insulating layer provides insulation between said underlying substrate topography and subsequently formed layers;
h) forming a third insulating layer superjacent and coextensive said exposed walls and inner bottom portion of said capacitor and said partially remaining first insulating layer; and
i) forming a second conductive layer superjacent and coextensive said third insulating layer.

42. A process as recited in claim 41, wherein said first insulating layer is planarized prior to said step of patterning and etching an opening into said first insulating layer.

43. A process as recited in claim 41, wherein said second insulating layer is a sacrificial layer that is planarized by chemical mechanical planarization.

44. A process as recited in claim 41, wherein said first and said second insulating layers are oxides.

45. A process as recited in claim 41, wherein said first insulating layer etch rate is a lower etch rate than said second insulating layer etch rate.

46. A process as recited in claim 45, wherein the etch rate ratio between said second insulating layer etch rate and said first insulating layer etch rate is a ratio of 2:1 or greater.

47. A process as recited in claim 45, wherein the etch rate ratio between said second insulating layer etch rate and said first insulating layer etch rate is a ratio of 4:1.

48. A process as recited in claim 41, wherein said first and said second conductive layers are doped polysilicon.

49. A process as recited in claim 48, wherein said doped polysilicon is formed by insitu doped chemical vapor deposition.

50. A process as recited in claim 41, wherein said first, said second and said third insulating layers are formed by chemical vapor deposition.

51. A process for fabricating a DRAM container storage capacitor on a silicon substrate having active areas, word lines and digit lines, said process comprising the following sequence of steps:

a) forming a blanketing first insulating layer, having a first etch rate, over said existing topography;

b) patterning and etching an opening into said first insulating layer, said opening thereby forming a container form;

c) forming a conformal first conductive layer superjacent said first insulating layer and said container form thereby lining said container form;

d) forming a blanketing second insulating layer, having a second etch rate, superjacent said first conductive layer;

e) removing said second insulating layer via chemical mechanical planarization until upper portion of said first conductive layer is exposed;

f) removing said exposed first conductive upper layer via chemical mechanical planarization until underlying said first insulating layer is exposed thereby separating said first conductive layer into individual said container storage capacitors having inner and outer walls;

g) removing said first and said second insulating layers such that said second insulating layer is completely removed thereby exposing the entire inner walls of said container storage capacitor and said first insulating layer is partially removed thereby exposing an upper portion of said outer walls of said container storage capacitor, wherein the partially remaining first insulating layer provides insulation between said underlying substrate topography and subsequently formed layers;

h) forming a third insulating layer superjacent and coextensive said exposed walls and inner bottom portion of said capacitor and said partially remaining first insulating layer; and

i) forming a second conductive layer superjacent and coextensive said third insulating layer.

52. A process as recited in claim 51, wherein said first insulating layer is planarized prior to said step of patterning and etching an opening into said first insulating layer.

53. A process as recited in claim 51, wherein said second insulating layer is a sacrificial layer conducive to said chemical mechanical planarization.

54. A process as recited in claim 51, wherein said first and said second insulating layers are oxides.

55. A process as recited in claim 51, wherein said first insulating layer etch rate is a lower etch rate than said second insulating layer etch rate.

56. A process as recited in claim 55, wherein the etch rate ratio between said second insulating layer etch rate and said first insulating layer etch rate is a ratio of 2:1 or greater.

57. A process as recited in claim 55, wherein the etch rate ratio between said second insulating layer etch rate and said first insulating layer etch rate is a ratio of 4:1.

58. A process as recited in claim 51, wherein said first and said second conductive layers are doped polysilicon.

59. A process as recited in claim 58, wherein said doped polysilicon is formed by insitu doped chemical vapor deposition.

60. A process as recited in claim 51, wherein said first, said second and said third insulating layers are formed by chemical vapor deposition.

* * * * *

61. A process for fabricating a capacitor on a substrate, said process comprising the steps of:

providing a first insulating layer on said substrate, said insulating layer having an opening therein forming a container;

forming a generally conformal first conductive layer over said first insulating layer and in said container;

forming a second insulating layer above said first conductive layer; and

removing at least a portion of said second insulating layer through use of chemical mechanical planarization until an upper portion of said first conductive layer is exposed.

62. The process of claim 61, further comprising the step of removing at least a portion of said upper portion of said first conductive layer until said first insulating layer is exposed.

63. The process of claim 61, wherein said second insulating layer is a sacrificial layer conducive to said chemical mechanical planarization.

64. The process of claim 61, wherein said first and said second insulating layers are oxides.

65. The method of claim 61, wherein said first insulating layer is subject to a first etch rate and said second insulating layer is subject to a second etch rate, and wherein said first etch rate is a lower etch rate than said second etch rate.

66. A process for fabricating a DRAM containing storage capacitor on a silicon substrate having an existing topography including active areas, word lines and digit lines, said process comprising the steps of:

providing a first insulating layer having a first etch rate, over said existing topography;

forming an opening into said first insulating layer, said opening thereby forming a container;

forming a conformal first conductive layer over said first insulating layer and said container, thereby lining said container;

forming a second insulating layer having a second etch rate, over said first conductive layer; and

removing said second insulating layer through use of chemical mechanical planarization until an upper portion of said first conductive layer is exposed.

67. The process of claim 66, further comprising the step of removing at least a portion of said upper portion of said first conductive layer until said first insulating layer is exposed, thereby forming a conductive container having inner and outer walls.

68. The process of claim 66, wherein said second insulating layer is a sacrificial layer conducive to said chemical mechanical planarization.

69. The process of claim 66, wherein said first and said second insulating layers are oxides.

70. The method of claim 66, wherein said first insulating layer etch rate is a lower etch rate than said second insulating layer etch rate.

71. A process for fabricating a DRAM container storage capacitor on a silicon substrate having an existing topography including active areas, word lines and digit lines, said process comprising the steps of:

providing a first insulating layer, having a first etch rate, over said existing topography;

forming an opening into said first insulating layer, said opening thereby forming a container;

forming a conformal first conductive layer over said first insulating layer and said container, thereby lining said container;

forming a second insulating layer, having a second etch rate, over said first conductive layer; and

removing said second insulating layer through use of chemical mechanical planarization until an upper portion of said first conductive layer is exposed;

removing at least a portion of said upper portion of said first conductive layer until said first insulating layer is exposed, thereby forming a conductive container having inner and outer walls.